## R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

## SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 15 lines 3-17, page 11 lines 12-23, page 8 lines 17-19, page 2 lines 19-22, page 14, lines 17-21, page 5 lines 21-24, page 7 line 15 - page 8 line 14, page 11 lines 3-14, page 9 lines 11-20 and FIGS. 3-5, 7, 11, 17 and 20, as originally filed. Thus, no new matter has been added.

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claim 13 under 35 U.S.C. §102(e) as being anticipated by Sherman '765 has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Sherman concerns a low power, high speed communication bus (Title).

Claim 13 provides a step for driving the signals unidirectionally on the input buses with a low swing. In contrast, the buses of Sherman appear to be bidirectional as illustrated in FIG. 1 of Sherman. Therefore, Sherman does not appear to disclose

or suggest a step for driving the signals unidirectionally on the input buses with a low swing as presently claimed.

Claim 13 provides a step for generating a plurality of intermediate signals by amplifying the signals on the input buses in response to a first clock signal at crosspoints. In contrast, the Office Action admits on page 9 that, "Sherman is however silent on teaching the crosspoint between the input and output busses amplifies the signal." Therefore, *prima facie* anticipation has not been established for admitting that the reference does not disclose or suggest all of the claim limitations.

Furthermore, Sherman appears to be silent regarding the controller 62 (asserted similar to the claimed crosspoints) generating an intermediate signal by amplifying input signals in response to a first clock signal as presently claimed. Therefore, Sherman does not appear to disclose or suggest all of the claim limitations.

Furthermore, despite the assertion on page 3 of the Office Action, the controller of Sherman do not appear to be a crosspoint. In particular, Sherman describes the controller in column 14, lines 46-50 as follows:

> The controller acts to process requests for access to the bus by the internal regions, grants access to the bus as needed, and controls the transfer of data and addresses between the high speed bus ports and the internal regions.

In contrast, Appendix A provides a common definition of a crosspoint switch from Universal Switching Corporation's website www.uswi.com:

> A switch which, when closed, connects the signal on an input bus to one or more output buses. Also referred to as a matrix switch or switching array.

One of ordinary skill in the art would not appear to understand a controller that processes requests for access to a bus to be similar to a switch that connects signals on an input bus to an output bus. Therefore, the assertion in the Office Action that the controller of Sherman is similar to the claimed crosspoint appears to be a conclusory statement. The Examiner is respectfully requested to either (i) provide evidence supporting the alleged similarity of the controller of Sherman to the claimed crosspoint or (ii) withdraw the rejection.

Claim 13 further provides a step for driving low swing signals on the output buses in response to the intermediate signals. In contrast, Sherman appears to be silent regarding intermediate signals within the alleged crosspoints. Therefore, Sherman does not appear to disclose or suggest a step for driving low swing signals on the output buses in response to the intermediate signals as presently claimed.

Claim 13 further provides a step for generating a plurality of output signals by sensing the low swing signals on the output buses. Despite the assertion on page 4 of the Office

Action, the text in column 10, lines 18-25 and column 14, lines 46-50 of Sherman appear to be silent regarding sensing signals on the output buses:

> Each port connected to the high speed bus may be provided with a VRef signal which is a stable reference voltage to which the other signals in the high speed bus are referenced. In accordance with the invention, the high speed bus may use low voltage swing signals (e.g., from 0.6 V to 1.65 V peak-to-peak). (Column 10)
>
> The controller acts to process requests for access to the bus by the internal regions, grants access to the bus as needed, and controls the transfer of data and addresses between the high speed bus ports and the internal regions. (Column 14)

Nowhere in the above text, or in any other section does Sherman appear to discuss **sensing signals** on the output buses. Therefore, the Examiner is respectfully requested to either (i) clearly identify where Sherman allegedly discusses sensing signals on output buses as presently claimed or (ii) withdraw the rejection.

## CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 8 and 9 under 35 U.S.C. §103(a) as being unpatentable over Mu et al., '213 (hereafter Mu) in view of Sherman has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claims 3-6 under 35 U.S.C. §103(a) as being unpatentable over Mu in view of Sherman and Krishnamurthy et al., '166 (hereafter Krishnamurthy) has been obviated in part by

appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claims 10-12, 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Mu in view of Sherman and Krishnamurthy and Karp '154 has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claims 13-16, 18 and 19 under 35 U.S.C. §103(a) as being unpatentable over Sherman in view of Mu has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claim 17 under 35 U.S.C. §103(a) as being unpatentable over Sherman in view of Mu and Lukes et al., '901 (hereafter Lukes) has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claim 22 under 35 U.S.C. §103(a) as being unpatentable over Mu in view of Sherman and Fletcher '466 has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claim 23 under 35 U.S.C. §103(a) as being unpatentable over Sherman in view of Mu and Fletcher has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Mu concerns a crossbar switch and method with crosspoint circuit (Title). Sherman concerns a low power, high speed communication bus (Title). Krishnamurthy concerns a tristate driver for integrated circuit interconnects (Title). Karp concerns multiconnection switching networks (Title). Lukes concerns a high speed differential output driver with increased voltage swing and predrive common mode adjustment (Title). Fletcher concerns an apparatus, method and system for a controllable pulse clock delay arrangement to control function race margins in a logic data path (Title).

Claim 1 provides a plurality of input buses, input signals on the input buses being driven at a low swing. In contrast, Mu only appears to consider signals V1 and V2 on lines 402 and 403 to be low-swing (see for example, column 6, lines 35-36 of Mu). Mu appear to be silent regarding a signal DATA on a line 410 (asserted similar to the claimed input bus) to be a low-swing signal. Therefore, Mu and Sherman, alone or in combination, do not appear to teach or suggest a plurality of input buses, input signals on the input buses being driven at a low swing as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify where Mu allegedly asserts that the signal DATA is a low-swing signal or (ii) withdraw the rejection.

Claim 1 further comprises a plurality of crosspoints, each comprising (i) a decoder configured to generate a first clock

signal and (ii) a repeater for selectively generating a respective one of the output signals in response to both a respective one of the input signals and the first clock signal. In contrast, both Mu and Sherman appear to be silent regarding a plurality of crosspoints, each comprising (i) a decoder configured to generate a first clock signal and (ii) a repeater for selectively generating a respective one of the output signals in response to both a respective one of the input signals and the first clock signal as presently claimed.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the alleged motivation provided in the Office Action is not credited to either reference or knowledge generally available as required by MPEP 2142. Therefore, the Examiner is respectfully requested to either (i) identify the source of the alleged motivation, and provide evidence if generally available knowledge or (ii) withdraw the rejection.

Furthermore, Mu and Sherman appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references

are allegedly analogous art under MPEP §2141.01(a) or (ii) withdraw the rejection.

Furthermore, the Office Action fails to provide any evidence of a reasonable expectation of success for the proposed combination/modification. In particular, no evidence exists that the transistors M3 and M4 or the inverter 415 of Mu would operate if the signal DATA were modified to be a low swing signal. Therefore, the Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success under MPEP 2142 or (ii) withdraw the rejection.

Claim 8 provides a plurality of amplifiers which amplify the output signals on the output buses, the amplifiers being clocked regenerative amplifiers having a gain using a positive feedback. In contrast, both Mu and Sherman appear to be silent regarding clocked regenerative amplifiers having a gain using a positive feedback as presently claimed. Claim 9 depends from claim 8. As such, claims 8 and 9 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 3 provides (i) an amplifier configured to generate an intermediate signal in response to both the respective input signal and the first clock signal and (ii) a low swing driver circuit configured to generate the respective output signal in response to the intermediate signal. In contrast, all of Mu, Sherman and Krishnamurthy appear to be silent regarding a

combination of an amplifier and a low swing driver at each crosspoint. Therefore, Mu, Sherman and Krishnamurthy, alone or in combination, do not appear to teach or suggest (i) an amplifier configured to generate an intermediate signal in response to both the respective input signal and the first clock signal and (ii) a low swing driver circuit configured to generate the respective output signal in response to the intermediate signal as presently claimed.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the alleged motivation provided in the Office Action is not credited to any reference or knowledge generally available as required by MPEP 2142. Therefore, the Examiner is respectfully requested to either (i) identify the source of the alleged motivation, and provide evidence if generally available knowledge or (ii) withdraw the rejection.

Furthermore, Mu, Sherman and Krishnamurthy appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400 and Krishnamurthy is in 326/83. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references are allegedly

analogous art under MPEP §2141.01(a) or (ii) withdraw the rejection.

Furthermore, the Office Action fails to provide any evidence of a reasonable expectation of success for the proposed combination/modification. In particular, no evidence exists that the single-ended input driver 205 of Krishnamurthy could accommodate the differential output generated by the transistors M3 and M4 of Mu. Therefore, the Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success under MPEP 2142 or (ii) withdraw the rejection.

Claim 4 provides that the amplifier is a clocked regenerative amplifier having a gain using a positive feedback. In contrast, all of Mu, Sherman and Krishnamurthy appear to be silent regarding a gain using a positive feedback. Therefore, Mu, Sherman and Krishnamurthy, alone or in combination, do not appear to teach or suggest a clocked regenerative amplifier having a gain using a positive feedback as presently claimed. As such, claim 4 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 5 provides a timing circuit which controls timing of the crosspoint switch from a second clock signal, the timing circuit including a delay which tracks a timing variation in the low swing driver circuit. Despite the assertion on page 6 of the Office Action, the arbitration unit of Mu (asserted similar to the

claimed timing circuit) does not appear to include a delay which tracks a timing variation in a low swing driver circuit (admitted missing from Mu on page 5 of the Office Action). Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation how Mu allegedly teaches that the arbitration circuit has a delay which tracks a timing variation of a low swing driver circuit not found in Mu or (ii) withdraw the rejection.

Claim 6 depends from claim 1 which is now believed to be allowable. As such, claim 6 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 10 provides a plurality of low swing drivers which drive a plurality of input signals to a plurality of input buses, each low swing driver driving a first pair of differential lines, one line driven high while the other line is pulled low. Despite the assertion on page 7 of the Office Action, Mu appears to be silent regarding (i) a line 410 (asserted similar to the claimed input bus) being differential and (ii) the signal DATA (asserted similar to the claimed input signals) being a low swing signal. In particular, Mu only appears to contemplate a signal V1 and V2 as differential low swing signals (see for example, column 6, lines 35-36 of Mu). Therefore, Mu, Sherman, Krishnamurthy and Karp, alone or in combination, do not appear to teach or suggest a plurality of low swing drivers which drive a plurality of input

signals to a plurality of input buses, each low swing driver driving a first pair of differential lines, one line driven high while the other line is pulled low as presently claimed.

Claim 10 further provides a plurality of precharge devices, each configured to precharge a respective one of the output buses to a mid-swing level by connecting the second pair of differential lines together. In contrast, all of Mu, Sherman, Krishnamurthy and Karp appear to be silent regarding precharging a differential low swing bus to a mid-swing level. Therefore, Mu, Sherman, Krishnamurthy and Karp, alone or in combination, do not appear to teach or suggest a plurality of precharge devices, each configured to precharge a respective one of the output buses to a mid-swing level by connecting the second pair of differential lines together as presently claimed.

Claim 10 further provides a plurality of crosspoints, each comprising (i) an amplifier which amplifies the respective input signal to generate an intermediate signal and (ii) a low swing driver which drives the respective output signal on one of the output buses in response to the intermediate signal. In contrast, all of Mu, Sherman, Krishnamurthy and Karp appear to be silent regarding a crosspoint having both an amplifier and a low swing driver. Therefore, Mu, Sherman, Krishnamurthy and Karp, along or in combination, do not appear to teach or suggest a plurality of precharge devices, each configured to precharge a

respective one of the output buses to a mid-swing level by connecting the second pair of differential lines together as presently claimed.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the alleged motivation provided in the Office Action is not credited to any reference or knowledge generally available as required by MPEP 2142. Furthermore, the use of four references against an independent claim hints at the claims being used as a template to choose the references. Therefore, the Examiner is respectfully requested to either (i) identify the source of the alleged motivation, and provide evidence if generally available knowledge or (ii) withdraw the rejection.

Furthermore, Mu, Sherman, Krishnamurthy and Karp appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400, Krishnamurthy is in 326/83 and Karp is in 340/825.8. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references are allegedly analogous art under MPEP §2141.01(a) or (ii) withdraw the rejection.

Furthermore, the Office Action fails to provide any evidence of a reasonable expectation of success for the proposed

combination/modification. In particular, no evidence exists that the single-ended input driver 205 of Krishnamurthy could accommodate the differential output generated by the transistors M3 and M4 of Mu. Therefore, the Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success under MPEP 2142 or (ii) withdraw the rejection.

Claim 11 provides a timing circuit which controls timing of the precharge devices and the crosspoints from a clock, the timing circuit including a delay which tracks timing variations in the low swing driver circuit. Despite the assertion on page 8 of the Office Action, the arbitration unit of Mu (asserted similar to the claimed timing circuit) does not appear to include a delay which tracks a timing variation in a low swing driver circuit (admitted missing from Mu on page 5 of the Office Action). Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation how Mu allegedly teaches that the arbitration circuit has a delay which tracks a timing variation of a low swing driver circuit not found in Mu or (ii) withdraw the rejection.

Claim 12 provides a first amplifier configured to generate a first half of the intermediate signal in response to both halves of the respective input signal and a second amplifier configured to generate a second half of the intermediate signal in response to both halves of the respective input signal. In

contrast, all of Mu, Sherman, Krishnamurthy and Karp appear to be silent regarding amplifiers responsive to both halves of an input signal. Therefore, Mu, Sherman, Krishnamurthy and Karp, alone or in combination, do not appear to teach or suggest a first amplifier configured to generate a first half of the intermediate signal in response to both halves of the respective input signal and a second amplifier configured to generate a second half of the intermediate signal in response to both halves of the respective input signal as presently claimed. As such, claim 12 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 20 provides a step for driving signals on the input buses at both edges of a first clock signal through a low swing on a pair of differential lines, one line driven high while the other line is pulled low. In contrast, all of Mu, Sherman, Krishnamurthy and Karp appear to be silent regarding driving data onto a bus on both edged of a clock signal. Therefore, Mu, Sherman, Krishnamurthy and Karp, alone or in combination, do not appear to teach or suggest a step for driving signals on the input buses at both edges of a first clock signal through a low swing on a pair of differential lines, one line driven high while the other line is pulled low as presently claimed.

Claim 20 further provides steps for (i) sensing the signals from the input buses and (ii) driving low swing signals on the output buses in response to both the signals and a second clock

signal at the crosspoints. In contrast, all of Mu, Sherman, Krishnamurthy and Karp appear to be silent regarding driving signal on output buses in response to a clock signal. Therefore, Mu, Sherman, Krishnamurthy and Karp, alone or in combination, do not appear to teach or suggest steps for (i) sensing the signals from the input buses and (ii) driving low swing signals on the output buses in response to both the signals and a second clock signal at the crosspoints as presently claimed.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the alleged motivation provided in the Office Action is not credited to any reference or knowledge generally available as required by MPEP 2142. Therefore, the Examiner is respectfully requested to either (i) identify the source of the alleged motivation, and provide evidence if generally available knowledge or (ii) withdraw the rejection.

Furthermore, Mu, Sherman, Krishnamurthy and Karp appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400, Krishnamurthy is in 326/83 and Karp is in 340/825.8. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references

are allegedly analogous art under MPEP §2141.01(a) or (ii) withdraw the rejection.

Furthermore, the Office Action fails to provide any evidence of a reasonable expectation of success for the proposed combination/modification. In particular, no evidence exists that the single-ended input driver 205 of Krishnamurthy could accommodate the differential output generated by the transistors M3 and M4 of Mu. Therefore, the Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success under MPEP 2142 or (ii) withdraw the rejection.

Claim 21 provides means for shorting together two lines in each of a plurality of output buses to precharge the lines to a mid-swing voltage. In contrast, all of Mu, Sherman, Krishnamurthy and Karp appear to be silent regarding shorting lines of output buses together. Therefore, Mu, Sherman, Krishnamurthy and Karp, alone or in combination, do not appear to teach or suggest means for shorting together two lines in each of a plurality of output buses to precharge the lines to a mid-swing voltage as presently claimed.

Claim 21 further provides a plurality of crosspoint means for (i) amplifying the signals from the input buses and (ii) driving low swing signals on the output buses by pulling up one of the lines and pulling down the other line. In contrast, FIG. 6 of Mu appears to contemplate that only pulling down is used to

generate a signal on a bus. Sherman and Krishnamurthy do not appear to cure the deficiency of Mu. FIG. 4 of Karp appears to illustrate amplifiers that both pull up and pull down. However, no motivation appears to exist to modify Mu with Karp since the precharge circuit 401 of Mu make the pullup capability of Karp redundant. As such, *prima facie* obviousness has not been established.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the alleged motivation provided in the Office Action is not credited to any reference or knowledge generally available as required by MPEP 2142. Therefore, the Examiner is respectfully requested to either (i) identify the source of the alleged motivation, and provide evidence if generally available knowledge or (ii) withdraw the rejection.

Furthermore, Mu, Sherman, Krishnamurthy and Karp appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400, Krishnamurthy is in 326/83 and Karp is in 340/825.8. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references are allegedly analogous art under MPEP §2141.01(a) or (ii) withdraw the rejection.

Furthermore, the Office Action fails to provide any evidence of a reasonable expectation of success for the proposed combination/modification. In particular, no evidence exists that the single-ended input driver 205 of Krishnamurthy could accommodate the differential output generated by the transistors M3 and M4 of Mu. Therefore, the Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success under MPEP 2142 or (ii) withdraw the rejection.

Claim 13 provide steps for (i) generating a plurality of intermediate signals by amplifying the signals on the input buses in response to a first clock signal and (ii) driving low swing signals on the output buses in response to the intermediate signals at the crosspoints. In contrast, both Sherman and Mu appear to be silent regarding step for amplifying and driving. Therefore, Sherman and Mu, alone or in combination, do not appear to teach or suggest steps for (i) generating a plurality of intermediate signals by amplifying the signals on the input buses in response to a first clock signal and (ii) driving low swing signals on the output buses in response to the intermediate signals at the crosspoints as presently claimed.

Furthermore, despite the assertion on page 9 of the Office Action, the amplifier 480 of Mu is not used at each crosspoint. In particular, FIG. 6 of Mu appears to contemplate (through the use of dashed lines) that there is only one precharge

circuit 401 at the top of a V1+V2 bus and one sense amplifier 480 at the bottom of the V1+V2 bus. Furthermore, the sense amplifier 480 of Mu does not appear to amplify the signal DATA (asserted similar to the claimed signal on the input bus). Therefore, Sherman and Mu, alone or in combination, do not appear to teach or suggest amplifying the signals on the input buses in response to a clock signal as presently claimed.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the Office Action does not provide any evidence of motivation to combine the references as required by MPEP 2142. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence of motivation under MPEP 2142 or (ii) withdraw the rejection.

Furthermore, Mu and Sherman appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references are allegedly analogous art under MPEP §2141.01(a) or (ii) withdraw the rejection.

Furthermore, the Office Action fails to provide any evidence of a reasonable expectation of success for the proposed

combination/modification. In particular, no evidence exists that the single-ended output of the sense amplifier 480 of Mu would drive the differential output signals of Sherman. Therefore, the Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success under MPEP 2142 or (ii) withdraw the rejection.

Claim 14 provides that the signals are amplified at the crosspoints by a clocked regenerative amplification having a gain using a positive feedback. In contrast, both Mu and Sherman appear to be silent regarding clocked regenerative amplifiers having a gain using a positive feedback as presently claimed. Claim 18 provides language similar to claim 14 As such, claims 14 and 18 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 15 provides a step for controlling timing of the crosspoint switch from a second clock signal such that data in the signals are driven onto the input buses on both edged of the second clock signal. In contrast, both Sherman and Mu appear to be silent regarding driving data onto buses on both edges of a clock signal. Therefore, Sherman and Mu, alone or in combination, do not appear to teach or suggest a step for controlling timing of the crosspoint switch from a second clock signal such that data in the signals are driven onto the input buses on both edged of the second clock

signal as presently claimed. As such, claim 15 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 16 provides that the signals on the input buses and the low swing signals on the output buses are differential signals. Despite the assertion on page 10 of the Office Action, Mu appears to be silent regarding the signal DATA (asserted similar to the signal on an input bus) being a differential signal. In particular, FIG. 6 of Mu appears to show that the signal DATA is a single-ended signal on one line 410. Therefore, *prima facie* obviousness has not been established and the rejection should be withdrawn.

Claim 19 depends from claim 13 which is now believed to be allowable. As such, claim 19 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 17 provides steps for (i) precharging a pair of differential line on each of the output buses to a mid-swing (ii) and driving the differential lines by push-pull driver circuits in response to the intermediate signals, one line driven high while the other line is pulled low. In contrast, all of Sherman, Mu and Lukes appear to be silent regarding precharging to a mid-swing and driving by push-pull driver circuits. Therefore, Sherman, Mu and Lukes, alone or in combination, do not appear to teach or suggest steps for (i) precharging a pair of differential line on each of the output buses to a mid-swing (ii) and driving the differential

lines by push-pull driver circuits in response to the intermediate signals, one line driven high while the other line is pulled low as presently claimed.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the Office Action does not provide any evidence of motivation to combine the references as required by MPEP 2142. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence of motivation under MPEP 2142 or (ii) withdraw the rejection.

Furthermore, Mu, Sherman and Lukes appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400 and Lukes is in 330/258. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references are allegedly analogous art under MPEP §2141.01(a) or (ii) withdraw the rejection.

Claim 22 provides a plurality of data-line-to-data-line precharge circuits that share charge between the differential data lines to a midpoint of voltage swing on the differential data lines. Despite the assertion on page 11 of the Office Action, the text in column 2, lines 19-35 of Fletcher appear to be silent regarding charge sharing between differential lines:

> More specifically, low-voltage-swing logic arrangements carry valid data signals on a pair of data "wires". A first data wire is used to carry a true value of the valid data signal and a second data wire is used to carry a complementary value of the same valid data signal. In a two-phase clocking arrangement, during a first clocking or pre-charging phase, both the data wires are pre-charged to a predetermined or pre-charge potential. At this point, the data wires do not contain any valid data or information. During a second clocking or evaluating phase, the potentials on the two wires may diverge in response to the information content of an input data signal. In particular, one data wire "evaluates" by transitioning toward an evaluation potential and the second data wire remains at the pre-charge potential, the low-voltage-swing logic arrangement then provides a valid data output signal based on the potential or voltage difference between the valid true and complementary data input signals. After the second clocking or evaluating phase, both data wires are again pre-charged to their pre-charge potential during a succeeding first clocking or pre-charge phase.

Nowhere in the above text, or in any other section does Fletcher appear to discuss charge sharing. Therefore, Mu, Sherman and Fletcher, alone or in combination, do not appear to teach or suggest a plurality of data-line-to-data-line precharge circuits that share charge between the differential data lines to a midpoint of voltage swing on the differential data lines as presently claimed. As such, claim 22 is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, the Office Action fails to establish clear and particular evidence of motivation to combine the references. In particular, the alleged motivation provided in the Office Action is not credited to any reference or knowledge generally available as required by MPEP 2142. Therefore, the Examiner is respectfully

requested to either (i) identify the source of the alleged motivation, and provide evidence if generally available knowledge or (ii) withdraw the rejection.

Furthermore, Mu, Sherman, and Fletcher appear to be non-analogous art. In particular, Mu is in US class/subclass 365/208 while Sherman is in 713/400 and Fletcher is in 327/392. In the absence of evidence to the contrary, the US classification system suggests that the references are non-analogous art. Claim 23 provides language similar to claim 22. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence why the references are allegedly analogous art under MPEP §2141.01(a) or (ii) withdraw the rejections of claims 22 and 23.

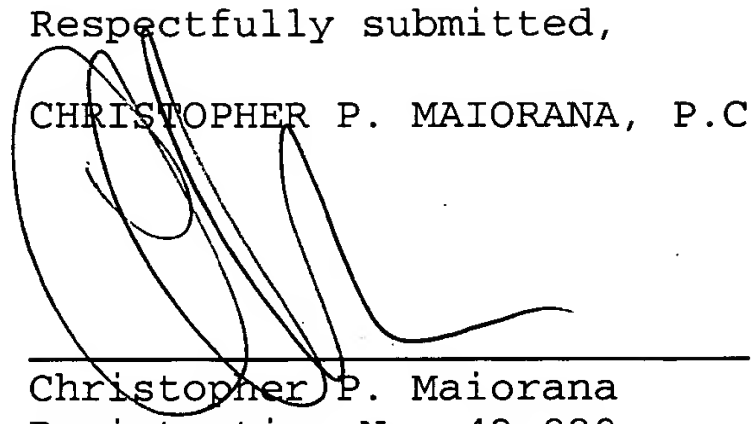
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Dated: April 11, 2005

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Appendix A
09/625,802


before failure. Life is dependent on the switched voltage, current, and power. Failure is usually when the contact resistance exceeds an end of life value. Typical failure mode is non-closure of the contact as opposed to a contact sticking closed.

- **Contact Potential** - A voltage produced between contact terminals due to the temperature gradient across the relay contacts, and the reed-to-terminal junctions of dissimilar metals. (The temperature gradient is typically caused by the power dissipated by the energized coil.) Also known as contact offset voltage, thermal EMF, and thermal offset. This is a major consideration when measuring voltages in the microvolt range. There are special low thermal relay contacts available to address this need. Special contacts are not required if the relay is closed for a short period of time where the coil has no time to vary the temperature of the contact or connecting materials (welds or leads).

- **Contact Rating** - The voltage, current, and power capacities of relay contacts under specified environmental conditions. See Carry Current and Switched Current.

- **Contact Resistance** - The resistance in ohms or milliohms across closed contacts. Also see Path Resistance.

- **Crosspoint Switch** - A switch which, when closed, connects the signal on an input bus to one or more output buses. Also referred to as a matrix switch or switching array.

- **Crosstalk/Crosstalk Isolation** - Unwanted interference in an output resulting from other input and output signals, measured in dB below the nominal signal level, and is expressed in decibels (dB) at a specified load impedance and over a specific frequency range or ranges. Also referred to as All Hostile or Hostile Crosstalk. See Channel Isolation.

- **Current Surge Limiting** - The circuitry necessary to protect relay contacts from excessive and possibly damaging current caused by capacitive loads.

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If you would like to submit additional terms and definitions, we encourage sending us email: eng@uswi.com

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